

ABSTRACT OF THE DISCLOSURE

A TFT memory 11 is provided with a polysilicon layer 22, wherein each region of the source 22a, the channel 22b and the drain 22c are formed on a substrate 21, and gate oxide films (insulating films) 23 and 25 are formed on the polysilicon layer 22; and a plurality of silicon particles 24 for trapping the charge of injected carriers are placed between the gate oxide films 23 and 25. Specifically, the gate oxide films comprise a first gate oxide film 23 and a second gate oxide film 25 formed on the first gate oxide film 23; the plurality of silicon particles 24 are located between the first gate oxide film 23 and the second gate oxide film 25, and the first gate oxide film 23 is formed in an extremely thin thickness.

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